Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously presented): A method for detecting process variations, the method comprising:

controlling count gate control by a first circuit;

generating at least one clock count by a second circuit; and

outputting results of the clock count by a third circuit.

Claim 2 (previously presented): The method of claim 1, wherein the controlling comprising:

activating a scan signal;

toggling a clock signal; and

setting a reset signal on.

Claim 3 (previously presented): The method of claim 2, wherein the controlling further comprising:

selecting an oscillator by activating and toggling the signals:

enabling the oscillator; and

setting the reset signal off.

Claim 4 (previously presented): The method of claim 2, wherein the controlling further comprising toggling the clock signal for a period of time.

Claim 5 (previously presented): The method of claim 1, wherein the generating further comprising:

outputting the count into a counter; and

reading the count into a scan chain.

Claim 6 (previously presented): The method of claim 4, wherein the toggling further comprising storing the output of the toggle in a counter.

Claim 7 (previously presented): The method of claim 5, further comprising toggling a clock for reading out the clock count.

Claim 8 (previously presented): The method of claim 1, further comprising communicating with a JTAG interface.

Claim 9 (previously presented): The method of claim 4, further comprising communicating with a JTAG interface.

Claim 10 (original): An apparatus to detect process variations comprising:

a first circuit to select a clock;

a second circuit connected to the first circuit to generate at least one clock count; and

a third circuit connected to the first circuit to output a result of the clock count.

Claim 11 (original): The apparatus of claim 10, wherein the first circuit comprises;

a scan signal; and

a clock signal, wherein the scan signal and the clock signal turn on at least one clock.

Claim 12 (original): The apparatus of claim 11, wherein the first circuit further comprises;

a reset signal; and

an enable signal, wherein the enable signal enables the at least one clock.

Claim 13 (original): The apparatus of claim 11, wherein the clock signal is toggled for a period of time.

Claim 14 (original): The apparatus of claim 13, wherein the second circuit further comprises outputting a count of the toggle.

Claim 15 (original): The apparatus of claim 14, wherein the third circuit comprises:

a counter; and

a scan chain, wherein the scan chain is connected to the counter.

Claim 16 (previously presented): The apparatus of claim 15, wherein the at least one count is input to the counter.

Claim 17 (original): The apparatus of claim 15, wherein the reset signal is input to the counter.

Claim 18 (original): The apparatus of claim 16, wherein the scan chain further comprises a read signal, wherein the read signal reads the count into the scan chain.

Claim 19 (original): The apparatus of claim 18, wherein the clock signal is toggled to read out the count from the scan chain.

Claim 20 (previously presented): The apparatus of claim 19, wherein the scan chain communicates with a JTAG interface.

Claim 21 (previously presented): A method for detecting process variations, comprising:

controlling count gate control by a first circuit to select a first oscillator;

generating a clock by the first oscillator in a second circuit;

counting the clock generated by the first oscillator by a third circuit;

outputting a count of the clock generated by the first oscillator by the third circuit;

selecting a second oscillator in the second circuit;

generating a clock by the second oscillator in the second circuit;

counting the clock generated by the second oscillator by the third circuit; and

outputting a count of the clock generated by the second oscillator by the third circuit.

Claim 22 (previously presented): The method of claim 21, further comprising:

selecting a third oscillator in the second circuit;

generating a clock by the third oscillator in the second circuit;

counting the clock generated by the third oscillator by the third circuit; and

outputting a count of the clock generated by the third oscillator by the third circuit.

Claim 23 (currently amended): An apparatus to detect process variations comprising:

a first circuit to control count gate control;

a first oscillator to generate a clock, wherein the first circuit is to select the clock generated by the first oscillator;

a ~~third~~ second circuit to count the clock generated by the first oscillator and to output the count of the clock generated by the first oscillator; and

a second oscillator to generate a clock, wherein the first circuit is to select the clock generated by the second oscillator, and the ~~third~~ second circuit is to count the clock generated by the second oscillator and is to output the count of the clock generated by the second oscillator.

Claim 24 (currently amended): The apparatus of claim 23, further comprising:

a third oscillator to generate a clock, wherein the first circuit is to select the clock generated by the third oscillator, and the ~~third~~ second circuit is to count the clock generated by the third oscillator and is to output the count of the clock generated by the third oscillator.

Claim 25 (canceled).

Claim 26 (previously presented): The apparatus of claim 24, wherein the first oscillator is a standard RING oscillator.

Claim 27 (previously presented): The apparatus of claim 24, wherein the second oscillator is an oscillator sensitive to the LTRAN process parameter.

Claim 28 (previously presented): The apparatus of claim 24, wherein the third oscillator is an oscillator sensitive to the RTRAN process parameter.

Claim 29 (previously presented): The apparatus of claim 23, wherein the first circuit includes a multiplexer.